CLAIMS

1. An apparatus comprising:

an analog circuit configured to generate a plurality of samples of an input signal in response to a plurality of phases of a reference clock; and

a digital circuit configured to generate an output signal and a clock signal in response to said plurality of samples and said plurality of phases, wherein said clock signal is aligned with said output signal.

2. The apparatus according to claim 1, wherein said analog circuit comprises a plurality of sampler circuits, each configured to generate one or more of said plurality of samples.

3. The apparatus according to claim 1, wherein said analog circuit comprises a multi-phase phase locked loop circuit configured to generate said plurality of phases.

4. The apparatus according to claim 1, wherein said clock signal is aligned with a predetermined point of a bit time of said output signal.

5. The apparatus according to claim 1, wherein said clock signal is aligned with a center of a bit time of said output signal.

6. The apparatus according to claim 1, wherein said digital circuit comprises one or more output circuit selected from the group consisting of a serial output circuit, a packed data output circuit, and a symbol data output circuit.

7. The apparatus according to claim 1, wherein said digital circuit is configured to align said clock signal by selecting one of said plurality of phases in response to an accumulated value.

8. The apparatus according to claim 7, wherein said digital circuit is configured to increment said accumulated value by a calculated bit width each time a phase is selected.

9. The apparatus according to claim 7, wherein said digital circuit is configured to align said clock signal by

selecting another one of said plurality of phases in response to a second accumulated value.

10. The apparatus according to claim 9, wherein said digital circuit is configured to increment said first and second accumulated values by a calculated bit width each time a phase is selected.

11. The apparatus according to claim 9, wherein said digital circuit is configured to generate said clock signal having two edges within a period of a predetermined one of said plurality of phases.

12. The apparatus according to claim 7, wherein said digital circuit is configured to determine a period of said clock signal based on said bit width.

13. The apparatus according to claim 1, wherein said output signal comprises one or more signal selected from the group consisting of a serial data signal, a packed data signal, a symbol data signal, a polarity signal and a strobe signal.

14. The apparatus according to claim 6, wherein said serial output circuit comprises a first-in-first-out (FIFO) memory having no resynchronization logic.

15. An apparatus comprising:

means for generating a plurality of samples of an input signal in response to a plurality of phases of a reference clock; and

means for generating an output signal and a clock signal in response to said plurality of samples and said plurality of phases, wherein said clock signal is aligned with said output signal.

16. A method for extracting clock and data information from an input signal comprising the steps of:

(A) receiving said input signal;

(B) generating a plurality of samples of said input signal in response to a plurality of phases of a reference clock; and

(C) generating an output signal and a clock signal in response to said plurality of samples and said plurality of phases, wherein said clock signal is aligned with said output signal.

17. The method according to claim 16, wherein step (B) comprises the sub-step of:

sampling said input signal by said plurality of phases of said reference clock.

18. The method according to claim 17, wherein step (C) further comprises the sub-step of:

selecting one of said plurality of phases as said clock signal in response to an accumulated value.

19. The method according to claim 18, wherein step (C) further comprises the sub-step of:

selecting another of said plurality of phases as said clock signal in response to a second accumulated value.

20. The method according to claim 19, wherein step (C) further comprises the sub-steps of:

decrementing said accumulated values by the number of phases in said plurality of phases; and

incrementing said accumulated values by a calculated bit width.